forming a metal layer on exposed portions of the amorphous silicon layer; and

crystallizing the amorphous silicon layer by applying thermal treatment and electric field to the resultant substrate,

wherein the thin film transistor having crystallized amorphous silicon layer is formed at each of the plurality of pixels minimizing metallic contamination in the channel region during crystallization.

REMARKS

By this Amendment, Applicant amends claims 1 and 14 and new claim 37 is added. Presently 37 claims are pending in the application.

In the current Office Action, the Examiner rejected claims 1-13 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Examiner asserts that in claim 1, line 6, there is no antecedent basis for "exposed portions of the amorphous silicon layer". Additionally, the Examiner asserts that in claim 14, line 11, --field—should replace "filed".

In response, the Applicant has amended claims 1 and 14 in accordance with the Examiner's assertions to obviate the rejection under § 112, second paragraph. Accordingly, the Applicant requests withdrawal of the rejection of claims 1-13 under § 112, second paragraph.

Applicant adds new independent claim 37. New claim 37 is allowable over the cited references in that the claim recites a number of elements including, minimizing metallic contamination in the channel region during crystallization. None of cited references, singly

or in combination, teaches or suggests at least these features of the invention. Accordingly, Applicant respectfully submits that claim 37 is allowable over the cited references.

The Examiner rejected claims 1-36 under 35 U.S.C. § 103, as being unpatentable over the combination of Maekawa (US Patent No. 6,066,547), Arai et al. (US Patent No. 5,576,222) and Seung-Ik Jun (Aepse '97) and/or Cristoloveanu et al. (SOI). This rejection is respectfully traversed.

As asserted in an earlier response and as supported by previous amendments to the claims, the claims directly or indirectly all recite that the substrate is a "glass" substrate and that "the thin film transistor having crystallized amorphous silicon layer is formed at each of the plurality of the pixels" in combination with "crystallizing the amorphous silicon layer."

Moreover, both Arai et al. and Cristoloveanu et al. concern a high temperature process, which would destroy the glass substrate of the claimed invention. For example, Arai et al. recites "producing an insulating layer on said solid phase growth layer by oxidizing surface of said solid phase growth layer at temperature 900°C - 1100°C." Such high temperature would completely destroy the glass substrate, which would teach directly against using a glass material. Also, Cristoloveanu et al. concerns silicon-on-insulator (SOI) which is also a high temperature process. Accordingly, Applicant respectfully submits that claims 1-36 are also allowable over the cited references.

In view of the foregoing, Applicant believes that this application is now in condition for allowance and therefore request favorable consideration and prompt allowance of the pending claims.

If the Examiner deems that a telephone conference would further the prosecution of this application, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0911.

Dated: October 16, 2002

Respectfully submitted,

By _____

Song K. Jung
Registration No.: 35,210
William D. Titcomb
Registration No.: 46,463
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500

Attachments:

Petition for Extension of Time
Additional Claim Fee Transmittal

MARKED-UP VERSION OF THE CLAIMS

1. (Twice Amended) A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising:

forming an amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a gate electrode on the amorphous silicon layer;

doping impurities of a first conductive type in the amorphous silicon layer;

forming a metal layer on [the] exposed portions of the amorphous silicon layer; and

crystallizing the amorphous silicon layer by applying thermal treatment and electric field to the resultant substrate,

wherein the thin film transistor having crystallized amorphous silicon layer is formed at each of the plurality of pixels.

14. (Twice Amended) A method of fabricating a thin film transistor for a liquid crystal display having a plurality of pixels comprising:

forming a first amorphous silicon layer as an active layer on a glass substrate;

forming a gate insulating layer and a second amorphous silicon layer as a gate electrode on the first amorphous silicon layer;

doping impurities of a first conductive type in the first and second amorphous silicon layers;

forming a metal layer on [the] doped portions of the first and second amorphous silicon layers; and

crystallizing the first and second amorphous silicon layers by performing heat treatment and applying electric [filed] <u>field</u> on the resultant substrate,

wherein the thin film transistor having crystallized amorphous silicon layer is formed at each of the plurality of pixels.